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Matrix Based Codes for Multiple Cell Error Detection and Correction in SRAM Cells Using Different Adders

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ABSTRACT:Transient multiple cell upsets (MCUs) are the data stored in the memory may be corrupted, when the memory is exposed to radiation environment. To prevent MCUs from causing data corruption, more complex error correction codes (ECCs) are widely used to protect memory, but the main problem is that they require complex encoder and decoder architecture and higher delay overheads. In this paper, decimal matrix code (DMC) based on divide symbols is proposed to enhance memory reliability with lower delay overhead. It utilizes decimal algorithm to obtain maximum error detection capability. The encode reuse technique (ERT) is proposed to minimize the area overhead of extra circuits without disturbing the whole encoding and decoding processes. ERT uses DMC encoder itself to be part of the decoder. Three different adders namely ripple carry adder, carry look ahead adder, and kogge stone adder are used in the DMC architecture and analyzed area, power and delay. Xilinx ISE 14.2 is used for the simulation outputs. The Simulation output shows that the DMC is more effective than existing codes in terms of Error Correction Capability. The Power consumption and delay is reduced in DMC. The Proposed DMC method has superior level of protection against Multiple Cell Upsets. The only drawback to the proposed scheme is that it requires more redundant bits for memory protection.

KEYWORDS: Error correction codes (ECCs), multiple cells upsets (MCUs), Encoder reuse technique (ERT); Decimal Matrix Code (DMC).

I. INTRODUCTION

As technology increases, soft error also increases. To reduce these soft errors we are using error correction codes (ECC).Different types of error correcting codes are widely used to protect memories against soft errors for years. The previous techniques having minimum error correction capability. The encoder and decoder circuits are more complex so it consumes more area and lower delay overhead. Decimal matrix code (DMC) based on divide symbol is proposed to provide enhance memory reliability. DMC utilizes decimal algorithm to detect errors therefore, error correction capability is maximized. Encoder reuse technique (ERT) is used to minimize the area overhead of extra circuits without disturbing the whole encoding and decoding processes. The DMC architecture with different types of adders is compared and analysis the area, power and delay. This is used to find the most efficient adder is used in the DMC. It reduces area, power and delay. This paper is divided in to following sections. Section 2 starts with literature review. Section 3 gives the implementation of decimal matrix code. Section 4 shows the work done. Simulation and results are explained in section 5. Finally, conclusion is explained in Section6.

II. LITERATURE REVIEW

The probability of soft errors in memory cells is increasing due to the scaling down of CMOS technology from micrometer to nanometre. This led to lowpower, low cost, high density and high speed integratedcircuits. Soft errors are major issue in the reliability of memory. It is a glitch in a semiconductor device. They are caused by a charged particle striking a semiconductor memory element [1].To prevent soft errors from causing corruption in the data stored error correction codes are used such as matrix code, hamming etc. Error correction codes are used to improve the memory protection and make the memory fault free. When error correcting code is used, data are encoded when written in a memory and data are decoded when read from memory [2]. These codes require more area, power and delay

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overheads since the encoding and decoding circuits are more complex. Different types of error correction codes are there.

- Single error- correction, double-error-detection double-adjacent error correction Code (SEC-DED-DAEC)
- Triple error correction code (TEC)
- Parallel Double Error Correcting code (DEC)
- Extended Hamming SEC-DED-TAED Code
- Reed Muller Code (RMC)
- Reed Solomon code (RSC)
- Punctured difference set (PDS)
- Build in current sensors (BICS)
- Matrix code (MC)
- Decimal Matrix Code (DMC)

The single error- correction, double-error-detection double-adjacent error correction (SEC-DED-DAEC) codes can detect and correct all adjacent double bit errors and a lower miscorrection probability for non-adjacent double bit errors [3]. It's simple to implement and provide low latency. The main disadvantage is it detects 2 bit errors and corrects 1 bit error. Triple error correction code (TEC) the decoders are simple to implement and reduce no: of additional bits in error correction and detection. The main drawback is that it detects and corrects 3 bit errors [4]. In parallel double error correcting code (DEC) detects up to 13 bit errors.DEC scheme reduces errors by 98.5% compared to conventional SEC-DED ECC [5]. Complexity of the decoders and the added latency is large in the circuit. Hamming codes are commonly used to protect memories or registers from soft errors. Multiple errors are not detected.Extended Hamming SEC-DED-TAED Codes detects adjacent errors which are caused by Multiple Cell Upsets (MCUs) in memories [6]. Memory area, power and speed will be the same as in previous techniques. It can detect and correct only 2bit errors. Reed Muller Code (RMC) is a linear error correcting code. It is used for high performance memory architecture. It Increases the performance and error tolerance. Area, power and access time are increased in this code [7]. Reed Solomon codes and punctured difference set (PDS) codes have been used to deal with MCUs in memories. But these codes require more area, power, and delay overheads since the encoding and decoding circuits are more complex in these complicated codes. Build in current sensors (BICS) are used to assist with single error correction and double error detection codes to provide protection against MCUs. The main disadvantage is that it can correct only two errors in a word. Matrix code combines with Hamming and Parity codes. It is a higher level error detection and correction method. MC is capable of correcting only two errors in all cases. The results obtained have shown that this approach have a lower delay overhead over other codes [8].

The DMC architecture with different types of adders is compared and analysis the area, power and delay. Different types of adders are

- Ripple carry adder
- Carry look ahead adder
- Kogge stone adder

The ripple carry adder is constructed by cascading full adder blocks in series. The carryout of one stage is fed directly to the carry-in of the next stage. For an n-bit parallel adder, it requires n full adders. The main drawback is not very efficient when large bit numbers are used and the delay increases linearly with the bit length. The carry look ahead adder (CLA) solves the carry delay problem by calculating the carry signals in advance, based on the input signals. The disadvantage of CLA is that the carry logic block gets very complicated for more than four bits. The kogge stone adder is a modification of carry look ahead adder [9]. The kogge stone adder has a lower fan out at each stage, it increases performance. The main disadvantage is wring congestion and large area.

III. DECIMAL MATRIX CODE

Decimal Matrix Code is proposed to assure reliability in the presence of MCUs with reduced performance overheads. A 32-bit word is encoded and decoded in this proposed method to detect and correct errors. It is based on divide symbol is proposed to provide enhanced memory reliability.

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A. System Architecture

In the proposed DMC, first, the divide-symbol and arrange-matrix ideas are performed. The N bit word is divided into k symbols of m bits and these symbols are arranged in a k1 × k2 2-D matrix. The DMC does not require changing the physical structure of the memory.

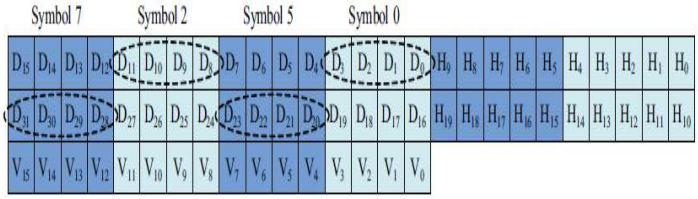

Fig. 1: 32 Bit DMC logical Organization

The cells from D0 to D31 are information bits. This 32-bit word has been divided into eight symbols of 4-bit. k1 = 2 and k2 = 4 have been chosen simultaneously. It should be mentioned that the maximum correction capability. Therefore, k and m should be carefully adjusted to maximize the correction capability and minimize the number of redundant bits.

B. System Design

First, during the encoding (write) process, information bits D are fed to the DMC encoder, and then the horizontal redundant bits H and vertical redundant bits V are obtained from the DMC encoder. When the encoding process is completed, the obtained DMC code word is stored in the memory. If MCUs occur in the memory, these errors can be corrected in the decoding (read) process. Due to the advantage of decimal algorithm, the proposed DMC has higher fault-tolerant capability with lower performance overheads. In the fault-tolerant memory, the Encoder Reuse technique is proposed to reduce the area overhead of extra circuits [10].

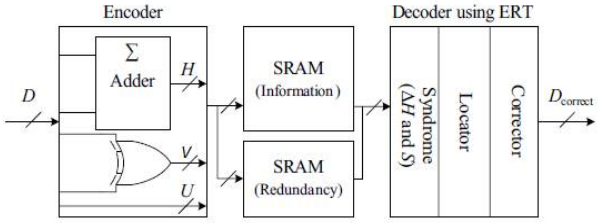

Fig. 2: Block Diagram of Decimal Matrix Code

C. Encoder

In the encoder section the cells from D0 to D31 are information bits. This 32-bit word has been divided into eight symbols of 4-bit. H0–H19 is horizontal check bits. H is produced by performing decimal integer addition of selected symbols per row. V0 through V15 are vertical check bits. V are obtained by binary operation among the bits per column. The horizontal redundant bits H can be obtained by decimal integer addition as follows:

$$H4H3H2H1H0 = D3D2D1D0 + D11D10D9D8$$
$$H9H8H7H6H5 = D7D6D5D4 + D15D14D13D12$$

And similarly for the horizontal redundant bits H14H13H12H11H10 and H19H18H17H16H15, where "+" represents decimal integer addition. For the vertical redundant bits V, we have

$$V0 = D0 \oplus D16 \quad (1)$$
$$V1 = D1 \oplus D17 \quad (2)$$

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and similarly for the rest vertical redundant bits. The encoder that computes the redundant bits using multi bit adders and XOR gates.

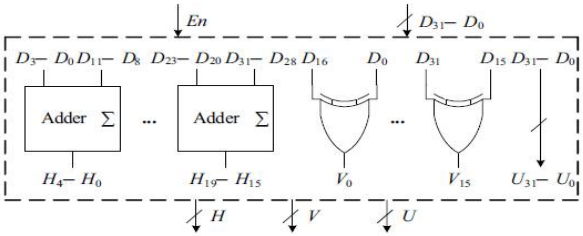

Fig. 3: 32 Bit DMC Encoder

D. DMC Decoder

The DMC decoder, having different sub modules and each executes a specific task in the decoding process: syndrome calculator, error locator, and error corrector. It can be observed from this figure that the redundant bits must be recomputed from the received information bits D' and compared to the original set of redundant bits in order to obtain the syndrome bits ΔH and S. Then error locator uses ΔH and S to detect and locate which bits some errors occur in. Finally, in the error corrector, these errors can be corrected by inverting the values of error bits. In the scheme, the circuit area of DMC is minimized by reusing its encoder. This is called the ERT. The ERT can reduce the area overhead of DMC without disturbing the whole encoding and decoding processes.

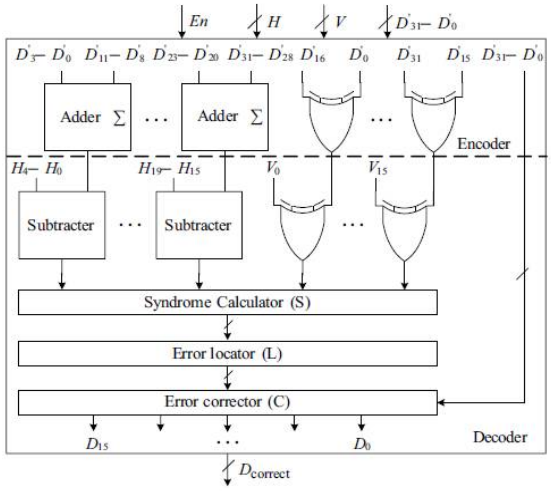

Fig. 4: 32 Bit DMC Decoder

To obtain a word being corrected, the decoding process is required. For example, first, the received redundant bits H4H3H2H1H'0 and V'0 −V'3 are generated by the received information bits D'. Second, the horizontal syndrome bits ΔH4H3H2H1H0 and the vertical syndrome bits S3 − S0 can be calculated as follows:

$$\Delta H4H3H2H1H0 = H4H3H2H1H'0 - H4H3H2H1H0$$
$$S0 = V'0 \oplus V0$$

and similarly for the rest vertical syndrome bits, where "–" represents decimal integer subtraction. When ΔH4H3H2H1H0 and S3 − S0 are equal to zero, the stored code word has original information bits in symbol 0 where no errors occur. When ΔH4H3H2H1H0 and S3 − S0 are nonzero, the induced errors are detected and located in symbol 0, and then these errors can be corrected by

$$D0correct = D0 \oplus S0$$

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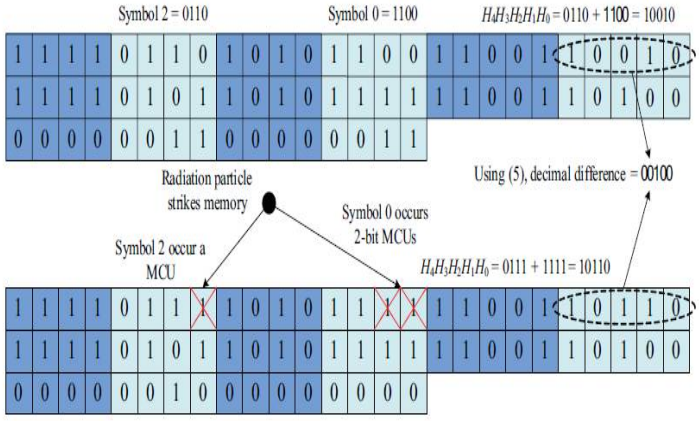

Fig. 5: Decimal Error Detection

IV. WORK DONE

32 bit decimal matrix code (DMC) is designed and analysed. Obtained maximum error detection and correction capability. Because of encoder reuse technique reduced the complexity of encoder and decoder circuit. Reduced area, power and delay overhead compared with the previous techniques. DMC with different adders are designed and analysed area, power and delay. Efficient adder is taken and implemented in the DMC.

V. RESULT AND DISCUSSION

Analysis were done on Xilinx ISE design suite 14.2.FPGA used is SPARTAN6, xc6slx45 cgs324 and speed -5 device is considered.

TABLE 1. ERROR CORRECTION CAPABILITY

Error Correcting Code	No. of Information bits	No. of Redundant bits	Error Correction Capability
DMC	32	36	5
Matrix Code	32	28	2
Hamming code	32	7	1

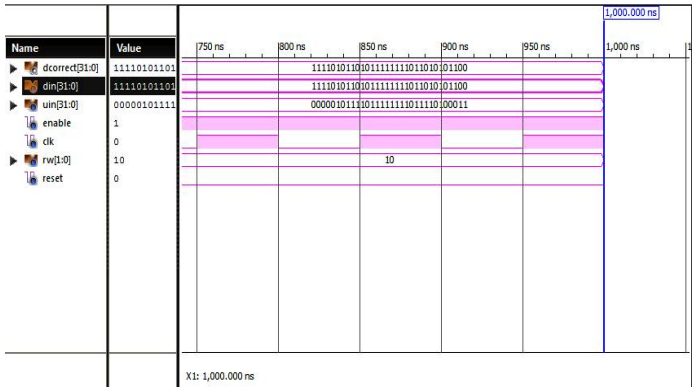

Fig. 6: Output waveform of DMC

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TABLE II: PERFORMANCE COMPARISON

Code	Device Utilization Summary			Delay(ns)	POWER (W)
	Slice reg	4 inputs	bounded IO		
DMC	196	165	100	9.066	0.037
Matrix code	164	291	100	14.548	0.105
Hamming code	1350	2682	100	17.133	0.163

Ripple carry adder, carry look ahead adder and kogge stone adders are combined with DMC and analysis area, power and delay. The obtained result is the delay is less and area is large in kogge stone adder. The power is same in all types of adders. Area is same in Ripple carry adder, carry look ahead adder.

TABLE III: DIFFERENT ADDERS DELAY ANALYSIS

Adders	Delay(ns)
Ripple carry adder	9.066
Carry look ahead adder	8.949
Kogge stone adders	6.362

VI. CONCLUSION

Error correction codes are used to improve the memory protection and make the memory fault free. The DMC utilized decimal algorithm to detect errors, so that more errors were detected and corrected. The DMC enhances the error correction capability up to 5 bits. The Simulation output shows that the DMC is more effective than existing Hamming and Matrix codes in terms of Error Correction Capability. Encoder reuse technique (ERT) is used to minimize the area overhead of extra circuits without disturbing the whole encoding and decoding processes. The Power consumption and delay is reduced in DMC. DMC with different adders are considered and the delay is less and area is large in kogge stone adder. The power is same in all types of adders. Area is same in Ripple carry adder, carry look ahead adder. The Proposed DMC method has superior level of protection against Multiple Cell Upsets.

REFERENCES

[1] E. Ibe, H. Taniguchi, Y. Yahagi, K. Shimbo, and T. Toba, “Impact of scaling on neutron induced soft error in SRAMs from an 250 nm to a 22 nm design rule,” *IEEE Trans. Electron Devices*, vol. 57, no. 7,pp. 1527–1538, Jul. 2010.

[2] D. Radaelli, H. Puchner, S. Wong, and S. Daniel, “Investigation of multi-bit upsets in a 150 nm technology SRAM device,” *IEEE Trans. Nucl. Sci.*, vol. 52, no. 6, pp. 2433–2437, Dec. 2005.

[3] M. Zhu, L. Y. Xiao, L. L. Song, Y. J. Zhang, and H. W. Luo, “New mix codes for multiple bit upsets mitigation in fault-secure memories, "micro *electron. J.*, vol. 42, no. 3, pp. 553–561, Mar. 2011.

[4] P. Reviriego, M. Flanagan, and J. A. Maestro, “A (64,45) triple error correction code for memory applications,” *IEEE Trans. Device Mater.Rel.*, vol. 12, no. 1, pp. 101–106, Mar. 2012.

[5] R. Naseer and J. Draper, “Parallel double error correcting code design to mitigate multi-bit upsets in SRAMs,” in *Proc. 34th Eur. Solid-State Circuits*, Sep. 2008, pp. 222–225.

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[6] A. Sanchez-Macian, P. Reviriego, and J. A. Maestro, "Haming SEC-DAED and extended hamming SEC-DED-TAED codes through selective shortening and bit placement," *IEEE Trans. Device Mater.Rel.*,to be published.

[7] C. Argyrides and D. K. Pradhan, "Improved decoding algorithm for high reliable reed muller coding," in *Proc. IEEE Int. Syst. On Chip Conf.*,Sep. 2007, pp. 95–98.

[8] C. Argyrides, D. K. Pradhan, and T. Kocak, "Matrix codes for reliable and cost efficient memory chips," *IEEE Trans. Very Large Scale Integr.(VLSI) Syst.*, vol. 19, no. 3, pp. 420–428, Mar. 2011.

[9] C. A. Argyrides, P. Reviriego, D. K. Pradhan, and J. A. Maestro,"Matrix-based codes for adjacent error correction," *IEEE Trans. Nucl.Sci.*, vol. 57, no. 4, pp. 2106–2111, Aug. 2010.

[10] Jing Guo, Liyi Xiao, Member, IEEE , Zhigang Mao, Member, IEEE , and Qiang Zhao "Enhanced Memory Reliability Against Multiple Cell Upsets Using Decimal Matrix Code", IEEE *Transactions On Very Large Scale Integration (Vlsi) Systems*, Vol. 22, No. 1, January 2014.